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Next-gen 3D transistors transform energy-efficient electronics

In a significant advancement for semiconductor technology, researchers at UC Santa Barbara have unveiled novel three-dimensional (3D) transistors utilizing two-dimensional (2D) semiconductors. Their approach paves the way for energy-efficient, high-performance electronics with unprecedented miniaturization potential.

“This breakthrough represents a major step toward the next generation of transistor technologies that can sustain the rapid progress of computing and artificial intelligence applications,” said Kaustav Banerjee, a professor of electrical and computer engineering and renowned expert in nanoelectronics and 2D materials. “By integrating atomically-thin 2D semiconductors into a 3D architecture, we have unlocked new possibilities for performance enhancement, transistor scalability and energy efficiency.”

Banerjee and his team’s work is published in the journal Nature Electronics.

Pushing the limits of transistor miniaturization

To enhance the performance of existing devices and enable advancements in newer technologies, the strategy of choice has been to miniaturize transistors — the fundamental components of modern electronics — to pack them in more densely and enable more operations on the chip with the same die size.

Indeed, some of the most significant advances in miniaturization have resulted in the design and development of strained-silicon and high-k/metal-gate field-effect transistors (FETs) that addressed scaling challenges and enhanced performance. However, in the case of the mainstream silicon technology, the transistors could get only so small before they hit limits to their performance, particularly in the realm of energy efficiency. These limitations, known as “short-channel effects,” arose in the form of subthreshold leakage currents and poor switching, making it difficult to downsize these transistors while keeping power consumption low.

Many of these limitations were overcome with the introduction of the Fin-FET more than a decade ago, a type of 3D architecture that wraps a “gate” around the channel that runs from the transistor’s source to its drain, mitigating short-channel effects while allowing for a smaller footprint. However, according to the authors, the downscaling of transistors beyond 10 nm channel length while keeping the power consumption low with good-performance is increasingly challenging, even for state-of-the-art Fin-FETs.

In this regard, the UCSB team’s study reveals that the enhanced electrostatics of 3D gate-all-around (GAA) structured transistors, when implemented with 2D semiconductors, could be used to realize ultimately scaled, few-nanometer channel length transistors with significantly boosted performance and energy efficiency. They have abbreviated these 3D GAA transistors as NXFETs, where N=nano, and X=sheet, fork or plate represent the topology of the channel stacking. Their study establishes how such transistors can be uniquely engineered with 2D semiconductors.

Unlocking the power of the nano-plate FET

In particular, the nano-plate FET architecture introduced in the study is shown to maximize the gains from the unique properties of atomically thin 2D materials like tungsten disulfide (WS_2). This novel architecture exploits lateral stacking of 2D layers, resembling a “stack of plates,” enhancing integration density by tenfold with iso-performance metrics.

“By leveraging the unique physical and quantum mechanical properties of 2D materials, we can overcome many of the limitations associated with conventional 3D transistors designed with silicon,” explained Banerjee. “Our simulations show that

the nano-plate transistors achieve significant improvements in energy efficiency and performance, with channel lengths scaled to sub-5nm dimensions.”

Cutting-edge tools for advanced design

The team utilized state-of-the-art simulation tools, including QTX — a quantum transport tool based on the non-equilibrium Green’s function framework — to evaluate the performance of their designs. This approach allowed them to model critical factors such as energy-band non-parabolicity, finite bandwidth, contact resistance and carrier mobility — measurements that describe the relationships between the material and the charge carriers (such as electrons) that travel through it. To provide accurate input parameters, the researchers used density functional theory, a theory developed in part by the late Walter Kohn, a UCSB physicist who won the 1998 Nobel Prize in Chemistry “for his development of density functional theory.”

“The combination of advanced quantum transport methods and practical considerations like non-ideal contact resistance and capacitances makes our framework both comprehensive and realistic,” said Arnab Pal, the lead author of the study.

Transforming CMOS scaling

The research findings indicate that 2D semiconductor-based 3D-FETs outperform their silicon counterparts in critical metrics such as drive current (the amount of current to operate a device) and energy-delay-product (the amount of energy needed for switching). The thinness of 2D materials minimizes device capacitance — which among other things, reduces power consumption — while their vertical stacking supports better scaling during fabrication.

“Our work not only demonstrates the potential of 2D materials but also offers a detailed blueprint for their integration into 3D transistor designs,” said Wei Cao, a co-author of the study. “This is a critical step forward for the semiconductor industry as it seeks to extend Moore’s Law.”

Looking ahead

With an eye on future advancements, the UCSB team plans to deepen collaborations with industry partners to accelerate the adoption of these technologies. They also aim to refine their models by incorporating additional real-world factors, such as defect scattering and self-heating, to support experimental validation.

“This research represents an exciting convergence of fundamental science and practical engineering,” Banerjee concluded. “We are committed to driving the transition of 2D semiconductors from the laboratory to real-world applications.”

The impact of this innovation extends beyond traditional computing, with potential applications in edge AI, flexible electronics and ultra-low-power devices for the Internet of Things. The findings also reinforce UC Santa Barbara’s leadership in advanced semiconductor research, continuing its legacy of pioneering breakthroughs in electronic and photonic technologies.

Research in this study was also conducted by Tanmay Chavan and Jacob Jabbour.

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